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EXAMINER	
PARIHAR, SUCHIN	

ART UNIT	PAPER NUMBER
2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,683	KARTSCHOKE ET AL.	
	Examiner	Art Unit	
	Suchin Parihar	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,12,14 and 16-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-10,12 and 16-20* is/are rejected.

7)☒ Claim(s) *6 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/605,683, amendment filed on 3/06/2006. Claims 1-10, 12, 14 and 16-20 are pending in this application. Claims 1-9, 12 and 16 are currently amended. The specification (i.e. abstract) is amended. Claims 11, 13 and 15 have been canceled.

2. Applicant's arguments filed 3/06/2006 have been fully considered but they are not persuasive. The applicable rejections from the prior office action are incorporated herein.

Claim Objections

3. Claim 1 is objected to because of the following informalities: With regard to step (c), this limitation recites the phrase "in response to the corresponding late mode being determined to be greater than zero in step (b)". However, the step in which the corresponding late mode margin is determined to be greater than zero is step (a). Therefore, Examiner suggests the following change to step (c) of claim 1: change the recitation "step (b)", found line 11 of claim 1, to –step (c)--.

4 Claim 4 is objected to because of the following informalities: This dependent claim lacks sufficient antecedent basis. Specifically, the last line of claim 4 includes the phrase "the timing cycle", wherein said phrase lacks sufficient antecedent basis. Although claim 1 provides intended use that involves the phrase "a timing cycle", said phrase has not been further recited in any of steps (a), (b) or (c), and therefore does not constitute part of an inventive step or recitation in the claims. Said phrase fails to

provide antecedent basis for any further recitation in the claims. Examiner suggests changing "the timing cycle" to –**a** timing cycle--.

5 Claim 4 is objected to because of the following informalities: The phrase "said delays" lacks sufficient antecedent basis. Claim 1 only refers to "a delay", and never to a plurality of delays.

6 Claims 17-20 are objected to because of the following informalities: "said delay" lacks sufficient antecedent basis; "said late mode margin" lack antecedent basis; and the phrase "of the corresponding one of said plurality of timing paths" is unclear in its intended meaning. Examiner suggests a replacement for the phrase "of the corresponding one of said plurality of timing paths", change said phrase to: –of the timing path in which the delay element is located--. Appropriate correction is required.

7 Claims 2-8, 10-15 and 17-20 are objected to because of the following informalities: These dependent claims use improper antecedent basis. The preamble of each of these dependent claims should appropriately relate back to its corresponding parent claim. For example, claim 2 begins: "**A** method according to claim 1... ". However, the method of which claim 2 is referring has already been established in claim 1. Therefore, the beginning of claim 2 should read --**The** method according to claim 1--. Claims 3-8, 10-15, and 17-20 also require corrections to their respective preambles.

Claim Objections Under 37 CFR 1.75

8 Claim 4 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper

dependent form, or rewrite the claim(s) in independent form. There is no mention of "timing cycle" in step (b) of claim 1. Therefore, claim 4 fails to limit the subject matter of claim 1 because claim 4 depends on subject matter (i.e. timing cycle) that is not present in the limitations of the parent claim. Examiner suggests changing "the timing cycle" to "**a** timing cycle".

Claim Rejections - 35 USC § 112

9 The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. **Claims 4 and 5 are rejected under 35 U.S.C. 112, second paragraph**, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. With respect to claim 4, the phrase "corresponding late mode margin minus a fraction of the timing cycle" does not correspond to the subject matter discussed on page 15 paragraph [0027] of Applicant's specification, wherein timing paths are moved, by a fraction of the timing cycle, from highest peak to lowest peak if that timing path is in a list of delayed timing paths (i.e. said phrase does not find support in Applicant's specification).

11. **Claims 16-20 are rejected under 35 U.S.C. 112, second paragraph**, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. With respect to claim 16, the omitted steps are: redistributing at least some of said plurality of timing paths within said timing cycle histogram. Claim 16 recites "in response to redistributing ....", but never recites apriori an actual step of redistributing.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. **Claims 1-3 and 16-18 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Kojima et al. (US PG Pub. 20030014724).

14. With respect to claims 1-3 and 16-18, Kojima teaches all elements of these claims as explained in their respective paragraphs below. Kojima fails to specifically teach the use of the following terms: "early mode" and "late mode". However, Kojima does teach the applicant's definitions of "early mode" and "late mode" as is described in the three paragraphs that follow:

> Although Kojima does not explicitly use the term "late mode", Kojima does use the term "timing slack", which the applicant refers to as "late mode margin" (Applicant's Specification, pg 9, paragraph [0020], line 2). Both the applicant and Kojima use the term "timing slack" to refer to a margin of time for further delaying timing signals. Applicant refers to "timing slack" on page 10 of the specification, in paragraph [0021], lines 1-3 (i.e. margin for delaying timing signals). Kojima refers to timing slack on page 4 in paragraph [0055] (i.e. "degree of allowance" for further delaying timing signals).

Although Kojima does not explicitly use the term "early mode", Kojima discusses a constraint time that closely fits the applicant's definition of "early mode" margin. Kojima discusses this constraint time on page 2 in paragraph [0025] (i.e. a maximum delay time that exceeds some maximum delay constraint time). Applicant discusses "early mode margin" and its definition on page 10 of the specification in paragraph [0021] (i.e. margin between time when element must be triggered [maximum-delay time] and some time later when element is actually triggered [exceeding constraint]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kojima by substituting such terms as "early mode" and "late mode" for the descriptions of the delay-time problems discussed in Kojima, because such modification is consonant with Applicant's disclosed specification definitions.

15. With respect to claim 1, Kojima teaches a method for reducing the magnitude of an overall instantaneous current draw (pg 7, paragraph [0120], i.e. reduce peak current) during a timing cycle in a synchronous integrated circuit having a plurality of timing paths (pg 7, paragraph [0120], i.e. a "plurality of flip-flop circuits" which may constitute a plurality of timing paths) each having a late mode margin associated therewith (i.e. an allowance, pg 1, paragraph [0011]) is obtained for each flip-flop circuit), comprising the steps of: (a) stepping through the plurality of timing paths (obtaining an allowance for each flip-flop circuit, i.e. path, pg 1, paragraph [0011]) so as to determine for each one of the plurality of timing paths whether or not the corresponding late mode margin is

greater than zero (using a useful skew, wherein a useful skew is the same as a late mode margin that is greater than zero, i.e. a useful skew is determine for all circuit paths –a useful skew is greater than zero –a zero skew is equal to zero, pg 1, paragraph [0007]); (b) in response to the corresponding late mode margin being determined to be greater than zero in step (a), adding a delay to the corresponding one of said plurality of timing paths (i.e. inserting a delay to a clock, pg 1, paragraph 0011; Kojima recognizes that a delay can only be inserted for those circuit paths with a useful skew i.e. margin greater than zero); and (c) in response to the corresponding late mode being determined to be greater than zero in step (b), inserting a delay element into the corresponding one of the plurality of timing paths, said delay element configured to induce said delay into that one of the plurality of timing paths (i.e. inserting a device having a delay, pg 10, claim 2).

16. With respect to claim 16, Kojima teaches: a plurality of timing paths resulting in a timing cycle histogram (i.e. timing change probability chart, which effectively shows when each circuit may change or draw current at a particular time, pg 7, paragraph [0122-0123]); and a plurality of delay elements distributed among said plurality of timing paths in response to redistributing at least some of said plurality of timing paths within said timing cycle histogram (i.e. overlapping skew boundaries of Figure 10 are used to determine when each circuit path should switch in order to reduce peak current draw, which may result in a redistribution of when each circuit timing path will turn on, pg 7, paragraph [0122]).

17. With respect to claim 2, Kojima teaches all the elements of claim 1, from which the claim depends, as described above. Kojima teaches a method wherein at least some of the plurality of timing paths each have early mode problems (pg 2, paragraph [0025], i.e. maximum delay time constraint violation – early mode), the method further comprising, prior to step (c), the step of fixing said early mode problems (pg 4, paragraph [0058], i.e. if constraint exists, adjust clock skew).

18. With respect to claim 3, Kojima teaches all the elements of claim 1, from which the claim depends, as described above. Kojima teaches a method wherein each one of the plurality of timing paths has a corresponding late mode margin (pg 4, par 55, i.e. time slack of each flip-flop circuit is obtained) and includes setting each corresponding delay to said corresponding late mode margin (pg 4, par 55, i.e. setting the delay of a flip-flop circuit to an optimal value of its late mode margin i.e. timing slack).

19. With respect to claim 17, Kojima teaches all the elements of claim 16, from which the claim depends, as described above. Kojima teaches an integrated circuit wherein each said delay is substantially equal to late mode margin of the corresponding one of said plurality of timing paths (pg 4, paragraph [0057], i.e. all flip-flop circuits are substantially at the center of the timing slack within a permissible range).

20. With respect to claim 18, Kojima teaches all the elements of claim 16, from which the claim depends. Kojima teaches: wherein at least one said delay is substantially equal to said late mode margin of the corresponding one of said plurality of timing paths minus a predetermined period (i.e. delay may be set to the difference between Dopti

[optimal value of timing slack –late mode margin] and a current Di [some predetermined period], pg 4, paragraph [0055]).

21. **Claims 7-10 and 12 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Kojima et al. (US PG Pub. 20030014724) in view of Kovacs et al. (US PG Pub. 20050050496).

22. With respect to claim 7, Kojima teaches all the elements of claim 1, from which the claim depends. Kojima fails to teach: the step of removing at least one timing path from said portion of the plurality of timing paths . However, Kovacs teaches: removing at least one timing path from said portion of the plurality of timing paths (pg 1, paragraph [0008], lines 6-10). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Kovacs into the method of Kojima because Kovacs suggests an improvement by removing the wires of a timing path if that timing path exceeds a threshold delay (Kovacs, pg 1, paragraph [0008], lines 6-10).

23. With respect to claim 8, Kojima in view of Kovacs teaches all the elements of claim 7, from which the claim depends. Kojima teaches: wherein at least some of the plurality of timing paths each have early mode problems (pg 2, paragraph [0025], i.e. maximum delay time constraint violation – early mode), the method further comprising, prior to step (c), the step of fixing said early mode problems (pg 4, paragraph [0058], i.e. if constraint exists, adjust clock skew).

24. With respect to claim 9, Kojima teaches a method for reducing the magnitude of an overall instantaneous current draw (pg 7, par 120, i.e. reduce peak current) during a timing cycle in a synchronous integrated circuit having a plurality of timing paths (pg 7,

paragraph [0120], i.e. a plurality of flip-flop circuits) each having a late mode margin (Figure 6, S402, i.e. obtaining an optimal value of timing slack for each register F/Fi), the instantaneous current draw having a profile that includes a peak defined by a portion of the plurality of timing paths (i.e. peak value caused by the simultaneous switching of flip-flop circuit paths, pg 1, paragraph [0007]) comprising the steps of: determining if the late mode margin of each one of the plurality of timing paths is greater than zero (using a useful skew, wherein a useful skew is the same as a late mode margin that is greater than zero, i.e. a skew is determined for all circuit paths –a useful skew is greater than zero –a zero skew is equal to zero, pg 1, paragraph [0007]); and for each one of the plurality of timing paths having a late mode margin greater than zero, determining a delay (i.e. a delay is added to a clock signal in order to reduce peak current; Kojima recognizes that a delay can only be added for those circuit paths with a non-zero skew margin, pg 1, paragraph [0014]) for that one of the plurality of timing paths in direct response to the determination of step (a), said delay being a function of the corresponding late mode margin (i.e. an allowance [late mode margin] is obtained in order to insert a delay to a clock, pg 1, paragraph [0011]). Kojima does not teach: (c) removing at least one timing path from said portion of the plurality of timing paths. However, Kovacs teaches: (c) removing at least one timing path from said portion of the plurality of timing paths (pg 1, paragraph [0008], lines 6-10). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Kovacs into the method of Kojima because Kovacs suggests an improvement by

removing the wires of a timing path if that timing path exceeds a threshold delay (Kovacs, pg 1, paragraph [0008], lines 6-10).

25. With respect to claim 10, Kojima in view of Kovacs teaches all the elements of claim 9, from which the claim depends. Kojima teaches a method wherein each delay is equal to the corresponding late mode margin (pg 4, paragraph [0057], i.e. all flip-flop circuits are substantially at the center of the timing slack within a permissible range).

26. With respect to claim 12, Kojima in view of Kovacs teaches all the elements of claim 9, from which the claim depends. Kojima teaches a method wherein at least some of the plurality of timing paths each have at least early mode problems (pg 2, paragraph [0025], i.e. maximum delay time constraint violation – early mode), the method further comprising the step of fixing said early mode problems (pg 4, paragraph [0058], i.e. if constraint exists, adjust clock skew).

Allowable Subject Matter

27. Claims 6 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

28. Claims 4, 5, 19 and 20 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

29. The following is a statement of reasons for the indication of allowable subject matter: With respect to claim 4, the prior art made of record fails to teach: setting each one of at least some of said delays to said corresponding late mode margin minus a

fraction of the timing cycle. With respect to claim 6, the prior art made of record fails to teach: setting each delay to said corresponding late mode margin minus said corresponding early mode margin. With respect to claim 14, the prior art made of record fails to teach: for each one of the timing paths having a late mode margin greater than zero and an early mode margin greater than zero, subtracting the early mode margin from the late mode margin. With respect to claim 19 and 20, the prior art made of record fails to teach: delay is substantially equal to the difference between said late and early mode margin of the corresponding one of said plurality of timing paths.

Response to Arguments

30. Applicant's arguments filed 3/26/2006 have been fully considered but they are not persuasive.

With regard to Claim Objections:

31. Applicant argues that changing the phrase "late mode margin of the corresponding one of said plurality of timing paths" to the Examiner's suggested change would alter the meaning of said phrase, which is not Applicant's intention. However, said phrase is still unclear with respect to the subject matter of the invention. Applicant's explanation of said phrase provides a clearer meaning of said phrase wherein Applicant states that: each of the delay elements has a delay that is a function of the late mode margin of the timing path in which it [the delay element] is located. Therefore, Examiner recommends a further amendment to claims 17-20 as recommended above under the Claim Objections section of this office action.

32. With respect to Applicant's arguments regarding the phrase "a timing cycle", Examiner points out that intended-use recitation does not provide antecedent basis for subject matter found in the limitations of the claims. With regard to currently amended claim 4, there is no antecedent basis for the phrase "the timing cycle". Examiner suggests amending this claim as described above in the Claim Objections Under 37 CFR 1.75 section of this office action.

33. With regard to Applicant's argument over the use of the indefinite article "A", Examiner points out that there is an identity between the subject matter of the dependent and independent claims; the identity lies in the **method** which applicant is further limiting. Also, none of the "numerous examples" of the Landis reference cited by Applicant correspond with Applicants' claims.

With regard to Claim Rejections Under 35 U.S.C. 103:

34. Applicant argues that Kojima is completely silent on stepping through a plurality of timing paths and assigning delays in direct response to this stepping through process. Also, Applicant states that Kojima appears to require timing paths to be analyzed in sets, rather than singly as in amended claim 1. Examiner disagrees with this assertion.

35. Although "stepping through the plurality of timing paths" is not directly recited in Kojima, the result of the stepping process is determining whether or not the corresponding late mode margin (i.e. useful skew value, timing slack, allowance, pg 1, paragraphs [0007;0011]) is greater than zero. Kojima recognizes that a useful skew [i.e. late mode margin] is one that is greater than zero. Adversely, Kojima recognizes

that zero-skew may exist wherein the skew is found to be zero (pg 1, paragraph [0007]). In response to Kojima requiring timing paths to be analyzed in sets, Examiner points out that Kojima simply states that each timing path, along with its groups of elements (i.e. flip-flops) attached therein, are analyzed in such a way that a delay is added to their clock signal(s) in an effort to reduce peak current. Examiner asserts that step (a) is implicit in the method of Kojima, and is sufficient to support a rejection under 35 U.S.C. 103(a).

36. Applicant argues that Kojima is completely silent on the steps of: determining if the late mode margin of each timing path is greater than zero, and if so, determining a delay in direct response to the determination that is a function of the late mode margin of that path, as recited in claim 9. Examiner disagrees with this assertion.

37. Kojima teaches the effects of useful skew, and how such an allowance (i.e. useful skew) can allow for delays to be inserted in an effort to avoid simultaneous switching of flip-flop circuits to reduce peak current (pg 1, paragraphs [0007] and [0011]). Therefore, it is within the scope of Kojima to determine whether the skew is useful (i.e. whether the late mode margin is greater than zero), and to determine a delay in direct response to this determination that is based on the late mode margin value (i.e. obtain an allowance in order to insert a delay into a clock (pg 1, paragraph [0011]). Examiner asserts these steps are implicit in the method of Kojima, and is sufficient to support a rejection under 35 U.S.C. 103(a).

38. Applicant argues that Kojima is completely silent on the step of: removing at least one timing path from the peak portion of a timing cycle histogram, as recited in claim 9 step (c). Examiner disagrees with this assertion.

39. First, Examiner does not believe that claim 9 recites this step, as Applicant has argued. Examiner interprets claim 9 step (c) as it reads: removing at least one timing path from said portion of the plurality of timing paths. In response to the argument, Examiner agrees that, in fact, Kojima is silent on step (c) as recited in claim 9. However, Kovacs teaches step (c) on page 1, paragraph [0008] (i.e. removing a wire [i.e. timing path] if that wire exceeds a threshold delay). The motivation to combine is described earlier in the office action in the Rejection paragraph for claim 9. Examiner asserts that this step is explicit in the method of Kovacs, and is sufficient to support a rejection under 35 U.S.C. 103(a).

40. Applicant argues that Kojima does not disclose: a plurality of delay elements distributed among the plurality of timing paths in response to redistributing at least some of the timing paths within a timing histogram, as recited in claim 16. Examiner disagrees with this assertion.

41. Examiner points out that Kojima teaches this step on page 1, paragraph [0011], wherein Kojima states that delays are inputted to clocks (i.e. "delay elements are distributed among the plurality of timing paths") to make a difference with respect to a change in the other clocks as to avoid a concentration of change in the clock (i.e. which effectively results in: "redistributing at least some of the timing paths within a timing

cycle histogram"). Examiner asserts that step (b) of claim 16 is implicit in the method of Kojima, and is sufficient to support a rejection under 35 U.S.C. 103(a).

42. Applicant argues that nothing in the Kojima et al./Kovacs et al. combination teaches removing timing paths from a peak region of a timing path histogram as required by the claims. Applicant also argues that Kojima does not disclose the use of histograms in connection with their method. Examiner disagrees with these assertions

43. First, there is not a claim requiring: removing timing paths from a peak region of a timing path histogram. However, Kovacs teaches: removing a timing path if the delay information indicates that the delay of that timing path exceeds a threshold delay. This step would improve the invention of Kojima by providing a way to reduce a timing path's contribution to peak current, wherein that path has no margin for added delay. That is, if a timing path cannot be redistributed on a timing path histogram by way of its non-zero delay margin, then there is no way to reduce the peak current that a specific timing path induces, unless that timing path is completely removed. Therefore, the motivation is provided by Kovacs, wherein Kovacs states that if a threshold delay is exceeded (i.e. if the useful delay margin has been exceeded), then that timing path can be removed to avoid the violation. Secondly, in response to Applicant's assertion that Kojima does not teach a timing path histogram: Kojima teaches: a plurality of timing paths resulting in a timing cycle histogram (i.e. timing change probability chart, which effectively shows when each circuit may change or draw current at a particular time, pg 7, paragraphs [0122-0123]). Examiner asserts that Kojima in view of Kovacs teaches the steps described, and is sufficient to support a rejection under 35 U.S.C. 103(a).

44. In summary, Applicant fails to place claims 1-20 in condition for allowance. Examiner therefore maintains the rejections of claims 1-18 under 35 U.S.C. 103(a).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suchin Parihar whose telephone number is 571-272-6210. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm. +If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is

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